



Replacement Sheet

1/11

150

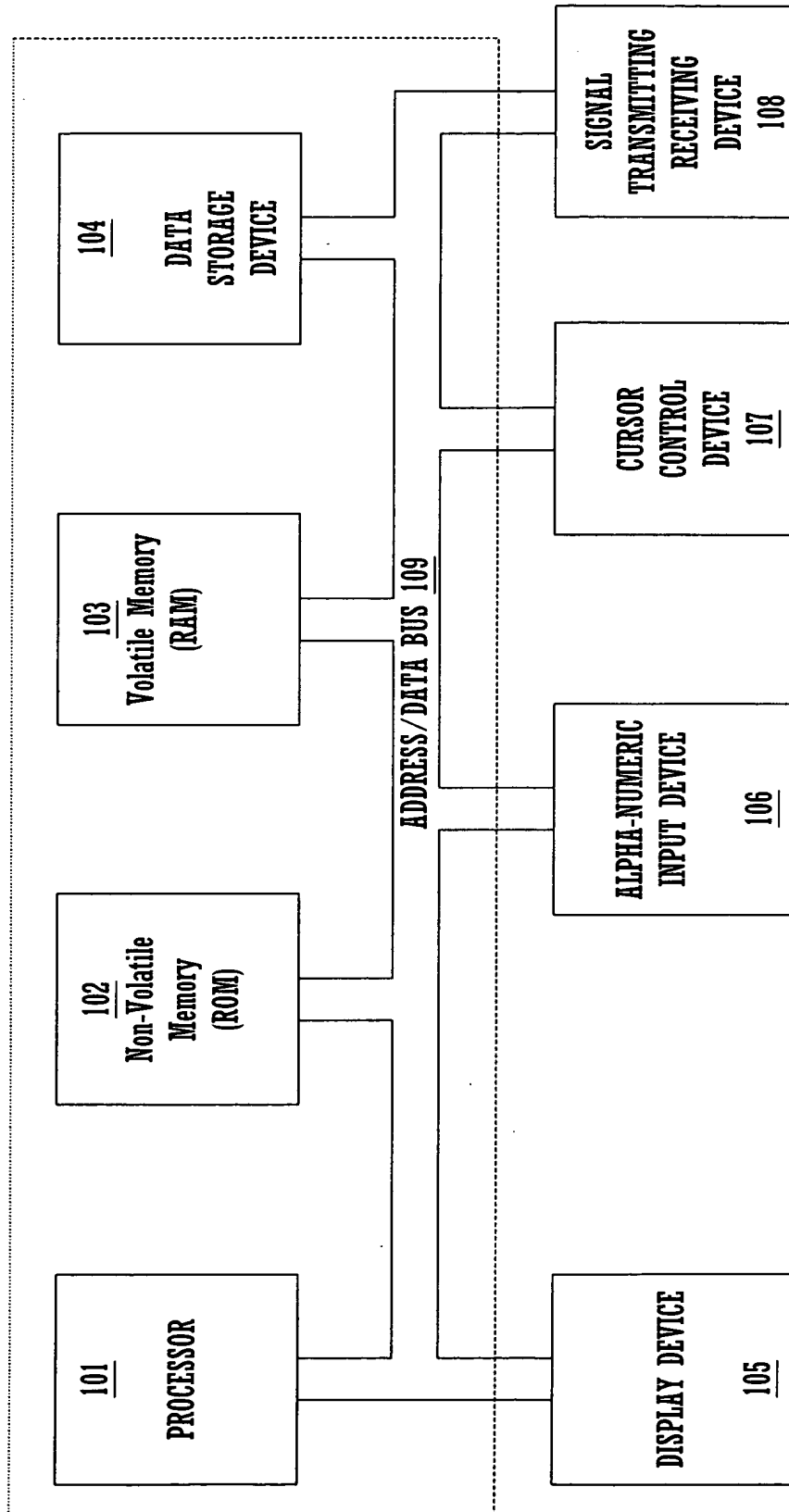


FIGURE 1

250

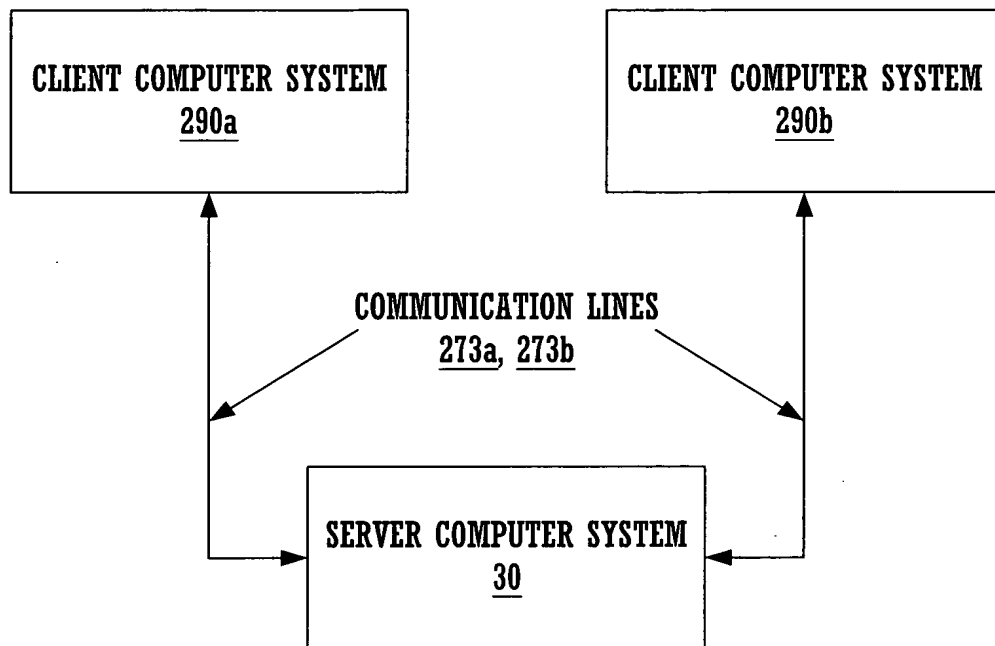


FIGURE 2

300

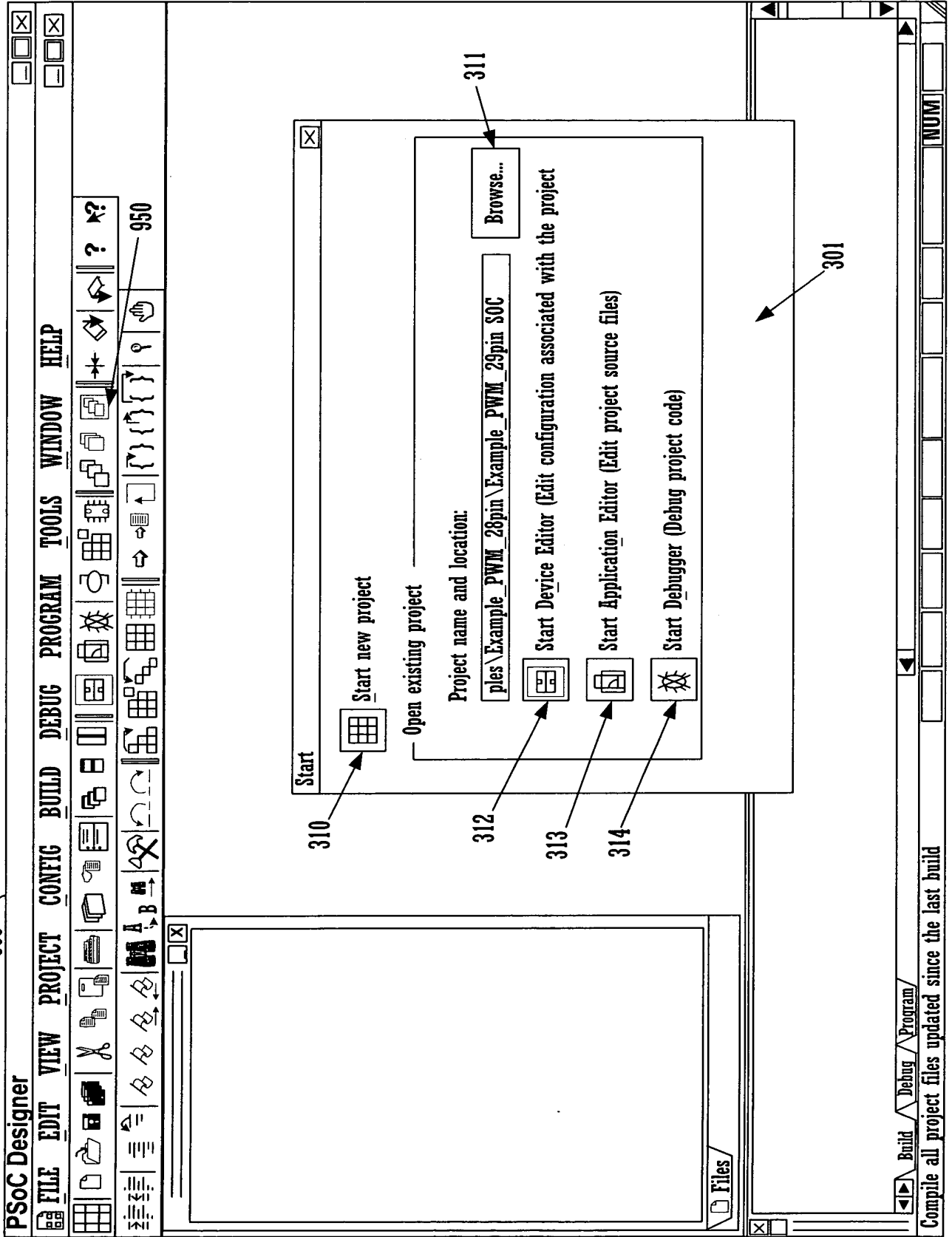


FIGURE
3

4/11

400

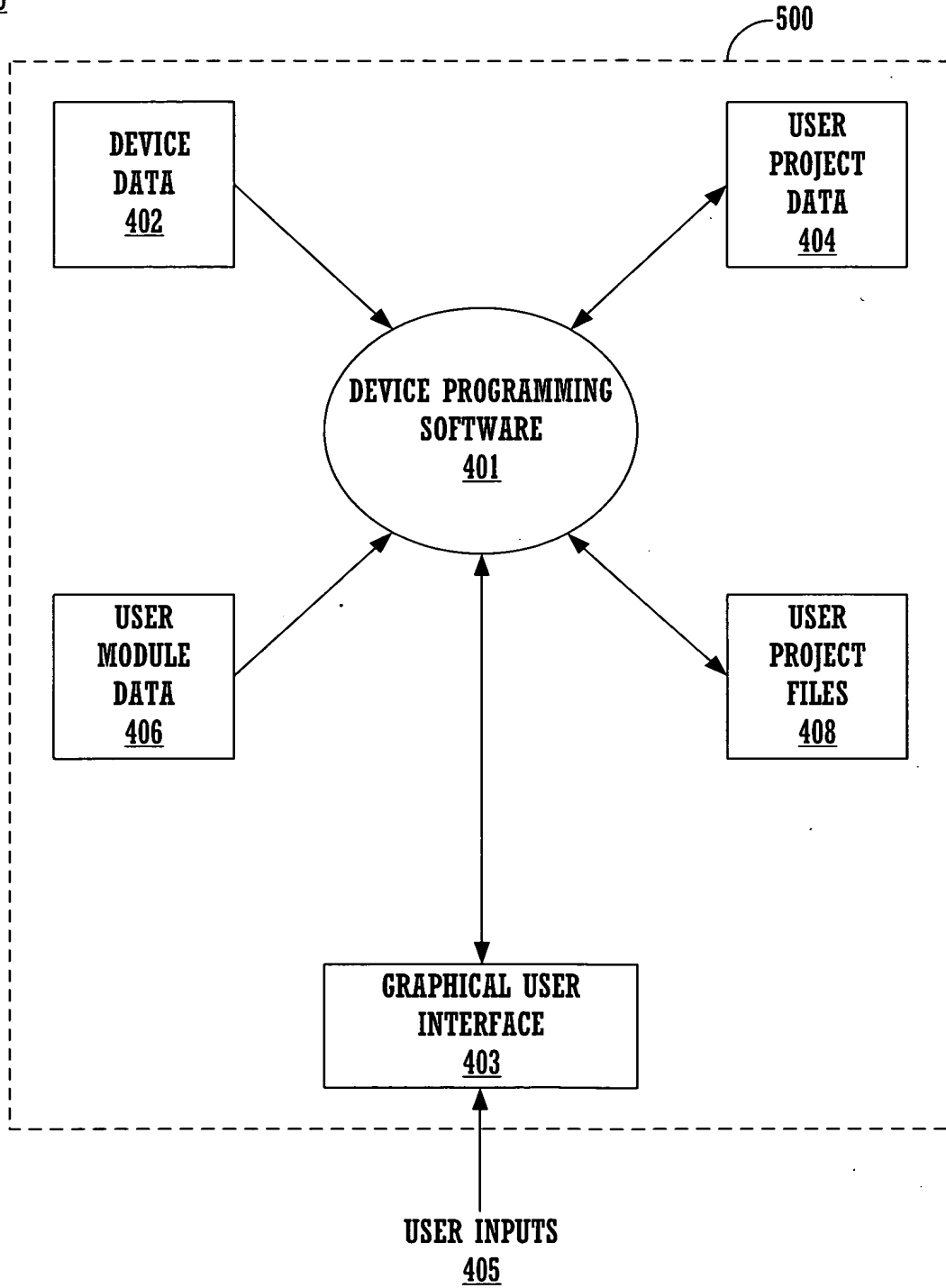
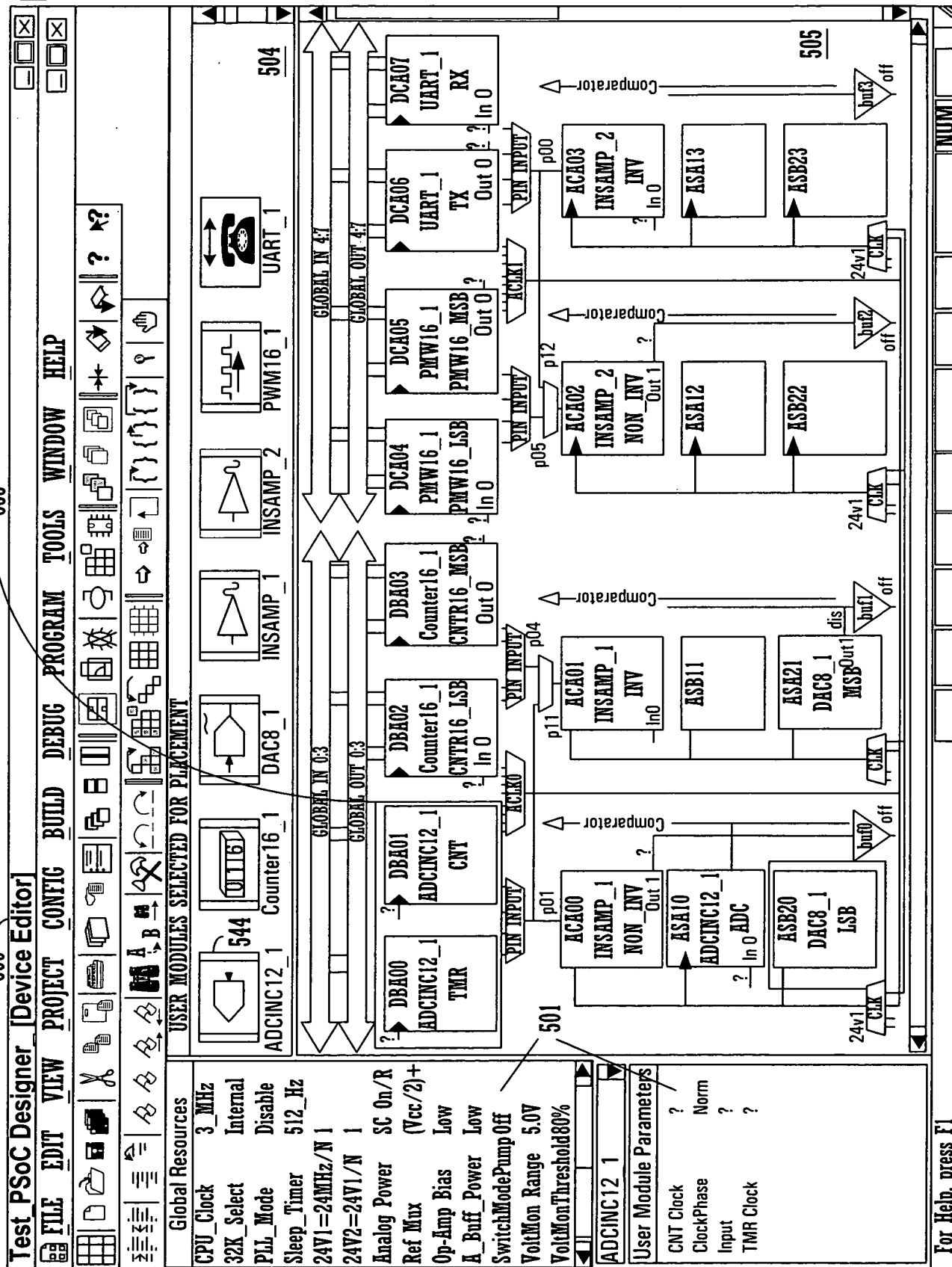


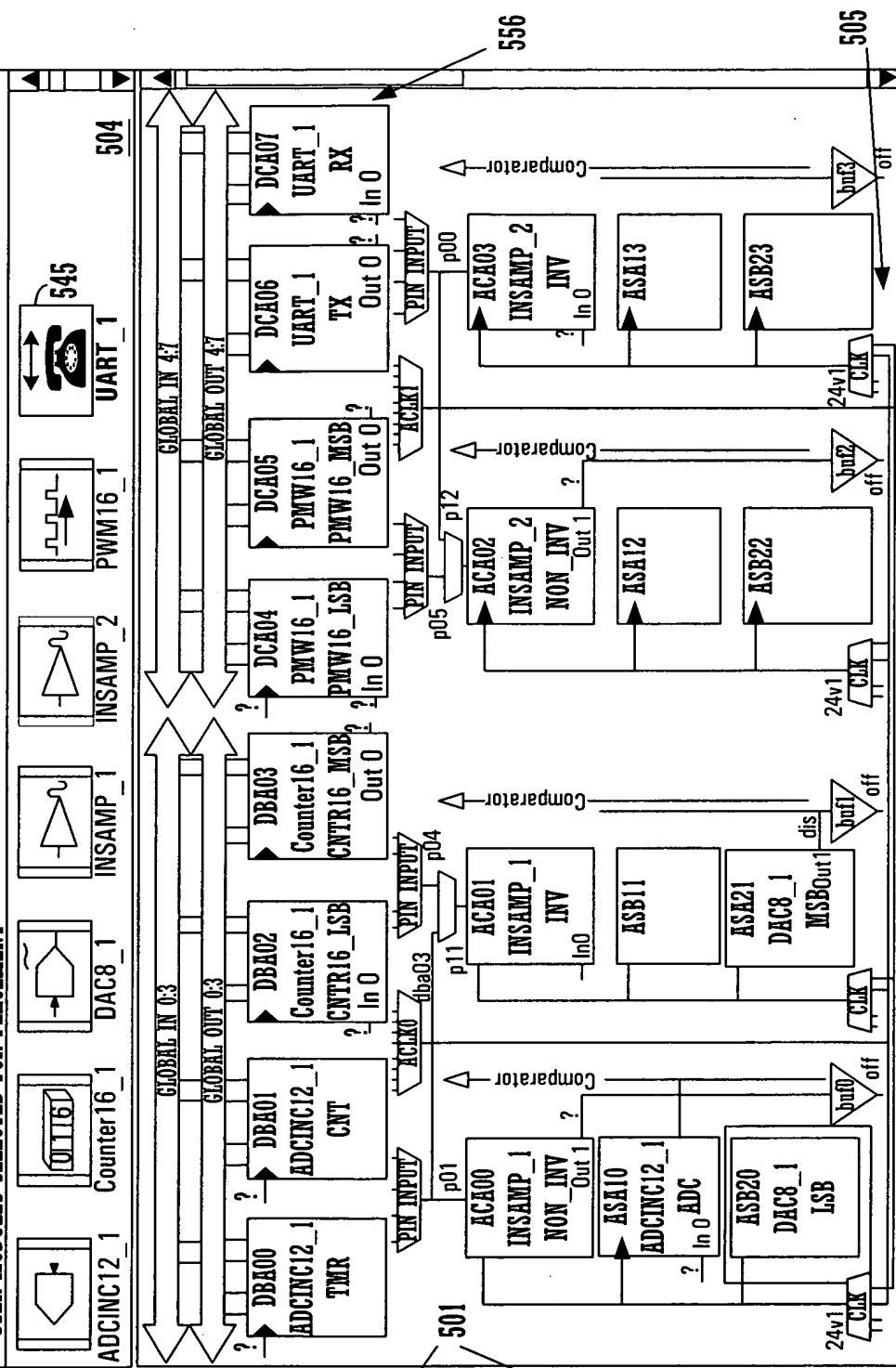
FIGURE 4

500

FIGURE 5



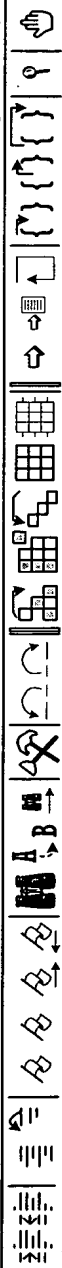
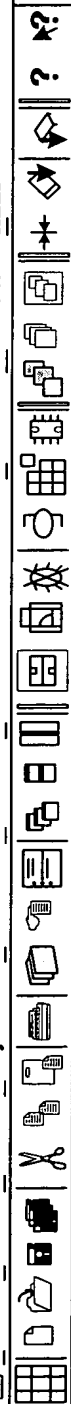
7/11



500

Test_PSoC Designer_ [Device Editor]

FILE EDIT VIEW PROJECT CONFIG BUILD DEBUG PROGRAM TOOLS WINDOW HELP



USER MODULES SELECTED FOR PLACEMENT

Global Resources

CPU_Clock 3_MHz
32K_Select Internal
PLL_Mode Disable
Sleep_Timer 512_Hz
24V1=24MHz/N 1
24V2=24V1/N 1
Analog_Power SC On/R
Ref_Mux (Vcc/2)+/-Ba
Op-Amp_Bias Low
A_Buff_Power Low
SwitchModePump Off
VotMonRange 5.0V
VotMonThreshold 80%

501

Port Drive

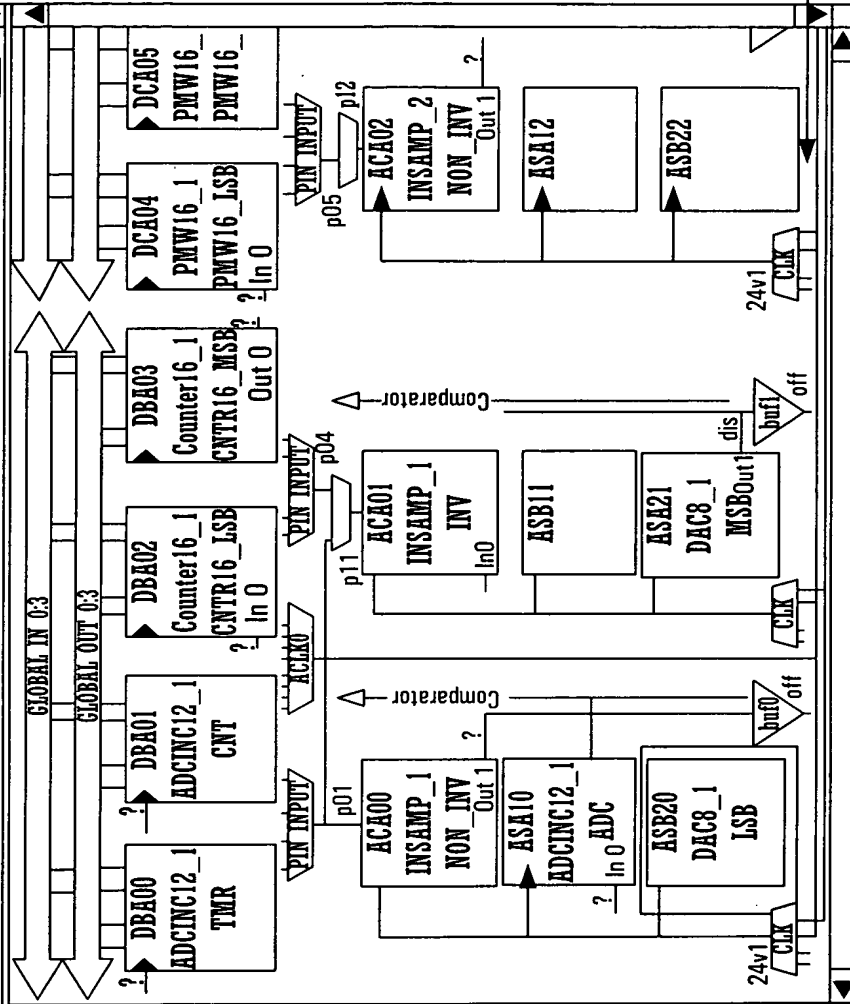
P0[0]	Pull Down
P0[1]	Pull Down
P0[2]	Pull Down
P0[3]	Pull Down
P0[4]	Pull Down
P0[5]	Pull Down
P0[6]	Pull Down
P0[7]	Pull Down
P1[0]	Pull Down
P1[1]	Pull Down
P1[2]	Pull Down
P1[3]	Pull Down
P1[4]	Pull Down
P1[5]	Pull Down
P1[6]	Pull Down

Switch to Pinout view

ADCINC12_1 Counter16_1 DAC8_1 INSAMP_1 INSAMP_2 PWM16_1 UART_1

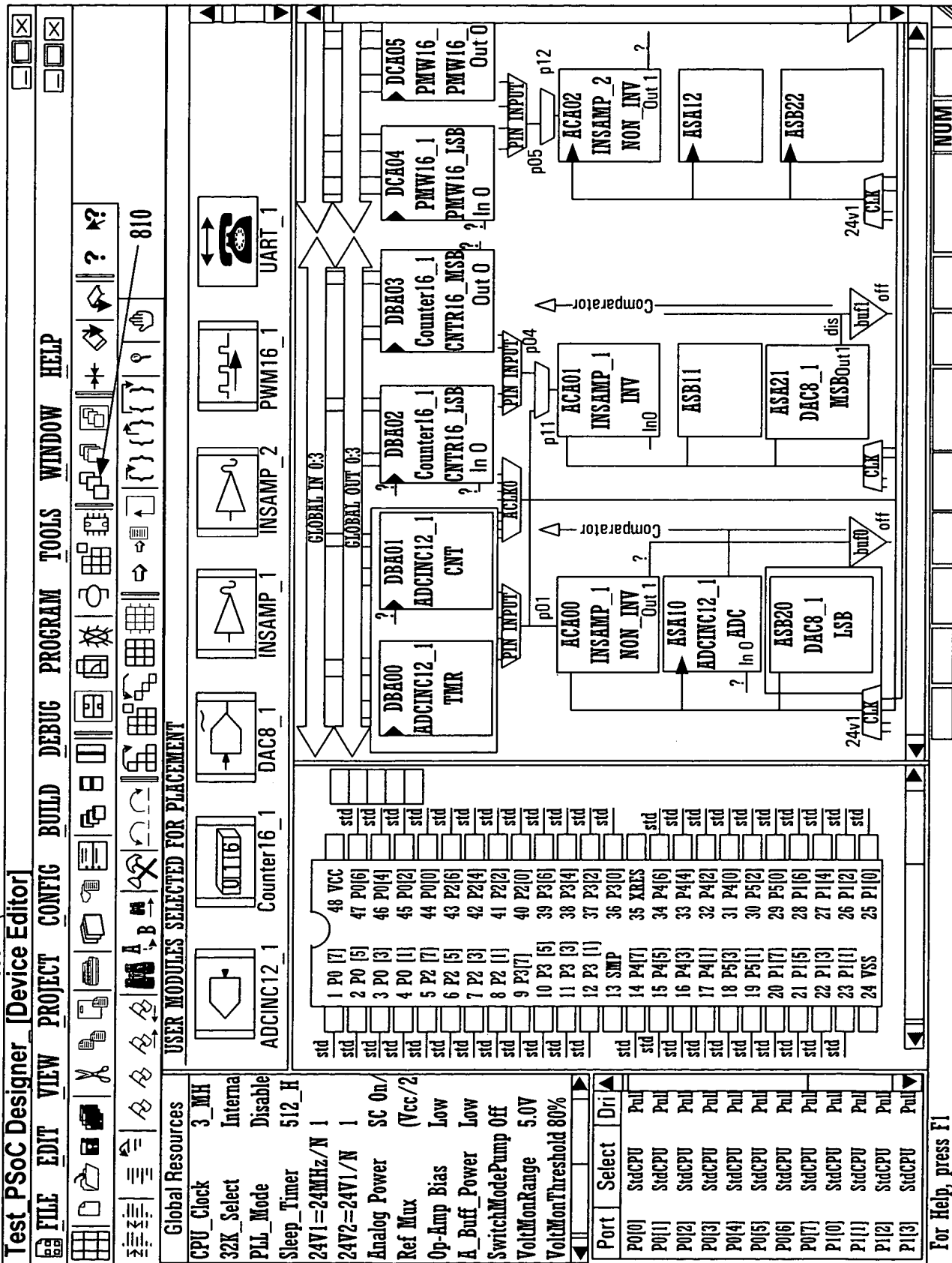
std	1 P0 [7]	48 VCC	std
std	2 P0 [5]	47 P0[6]	std
std	3 P0 [3]	46 P0[4]	std
std	4 P0 [1]	45 P0[2]	std
std	5 P2 [7]	44 P0[0]	std
std	6 P2 [5]	43 P2[6]	std
std	7 P2 [3]	42 P2[4]	std
std	8 P2 [1]	41 P2[2]	std
std	9 P3[7]	40 P2[0]	std
std	10 P3 [5]	39 P3[6]	std
std	11 P3 [3]	38 P3[4]	std
std	12 P3 [1]	37 P3[2]	std
std	13 SMP	36 P3[0]	std
std	14 P4[7]	35 XRES	std
std	15 P4[5]	34 P4[6]	std
std	16 P4[3]	33 P4[4]	std
std	17 P4[1]	32 P4[2]	std
std	18 P5[3]	31 P4[0]	std
std	19 P5[1]	30 P5[2]	std
std	20 P1[7]	29 P5[0]	std
std	21 P1[5]	28 P1[6]	std
std	22 P1[3]	27 P1[4]	std
std	23 P1[1]	26 P1[2]	std
std	24 VSS	25 P1[0]	std

506

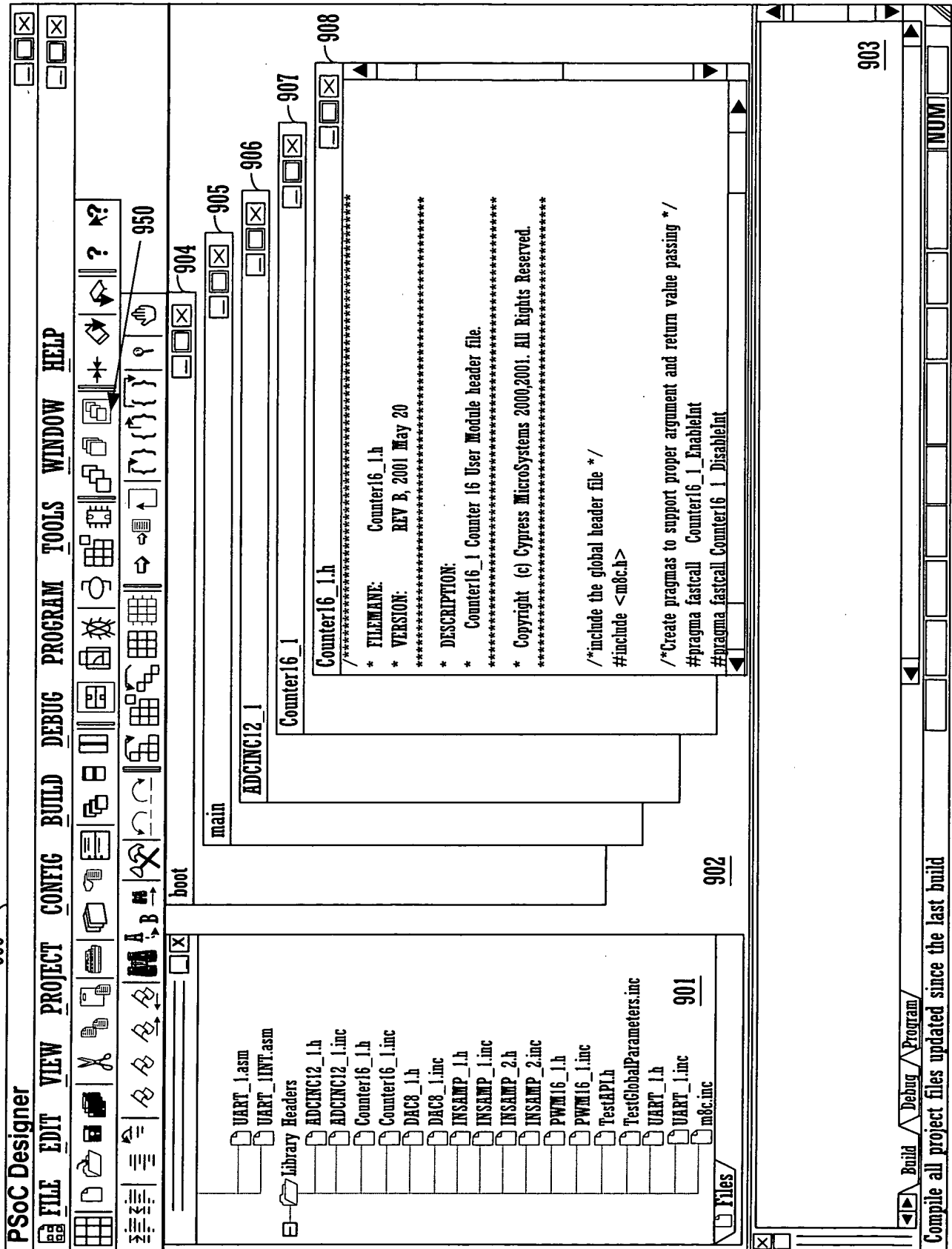


505

FIGURE 7



900



11/11

1000

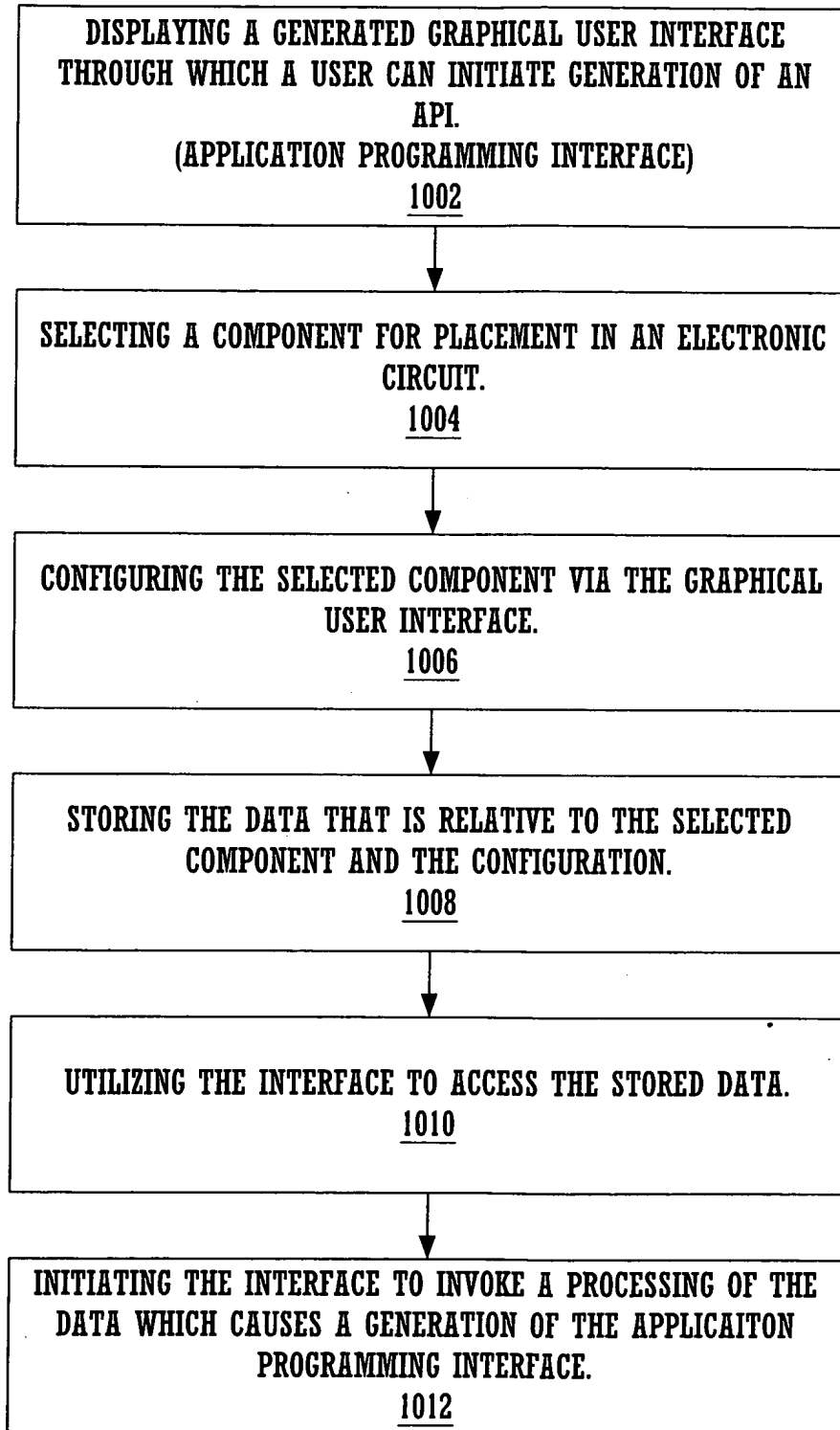


FIGURE 10